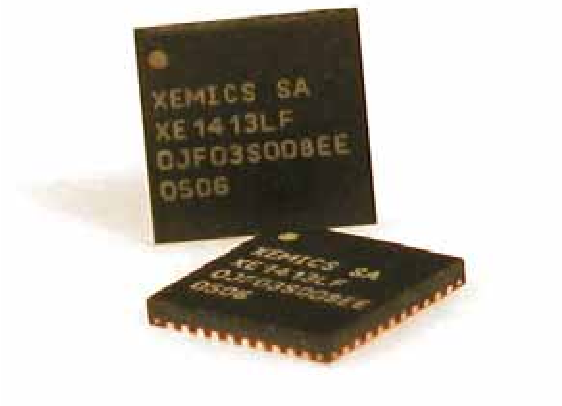
EasyBlue



XE1413

1.8V Ultra Low Power Bluetooth® RF Transceiver

GENERAL DESCRIPTION

The XE1413 is the next generation of ultra low powered, fully integrated single-chip Bluetooth radio transceiver solutions. Fully compliant with Bluetooth Specification v1.2, the XE1413 offers performances tailored for extremely low power operation in handsets, headsets, and other power-sensitive applications.

Transmitter output power is +2 dBm, while receiver sensitivity is –85 dBm. The frequency range allows operation in all 2.4 GHz Industrial, Scientific, Medical (ISM) band regulatory jurisdictions.

Fabricated in a Silicon-Germanium (SiGe) Bi-polar Complementary Metal Oxide Semiconductor (BiCMOS) process, the XE1413 is a state-of-the-art mixed signal device mounted in a tiny, low profile 6 x 6 x 0.75 mm, 40-pin TQFN green package.

APPLICATIONS

- ISM 2.4 GHz frequency band
- Personal wireless connectivity
- Cellular phones, handsets, headsets, earpieces
- PDAs, palm-top computers
- PC and laptop computers

ORDERING INFORMATION

Extended Part Number	Description
XE1413I068TR LF	2.4 GHz Bluetooth Transceiver

FEATURES

- Fully integrated single-chip transceiver with on-chip VCO, synthesizer, PA, LNA, image-reject down-converter, IF filters, RSSI, and demodulator for the ISM 2.4 GHz band
- Class 2 and 3 Bluetooth v1.2 compliant
- Typical receive sensitivity of –85 dBm at antenna
- Low voltage supply (1.8 V)
- Two internal voltage regulators (1.8 V and 1.5 V)
- Peak transmit current = 19 mA at maximum power
- Peak receive current consumption = 24 mA
- Peak transmit current = 11 mA at –10 dBm
- Low power timing clock mode (15 µA)
- Power-down current consumption <5 µA
- Temperature range of –40 to +85 °C is compliant with the Bluetooth specification
- Digital crystal frequency error compensation up to ±36 ppm
- Programmable transmit power control over 26 dB range with 2 dB steps
- High efficiency direct modulation transmitter using $\Delta\Sigma$ fractional-N synthesizer
- Low phase noise and closed loop PLL transmitter
- Integrated PLL-based FSK digital demodulator. No external component required
- High reliability, high yield SiGe BiCMOS process with low multiplicative 1/f noise
- TQFN 40-pin, 6 x 6 package, 0.5 mm pitch, lead-free

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1 CIRCUIT BLOCK DIAGRAM

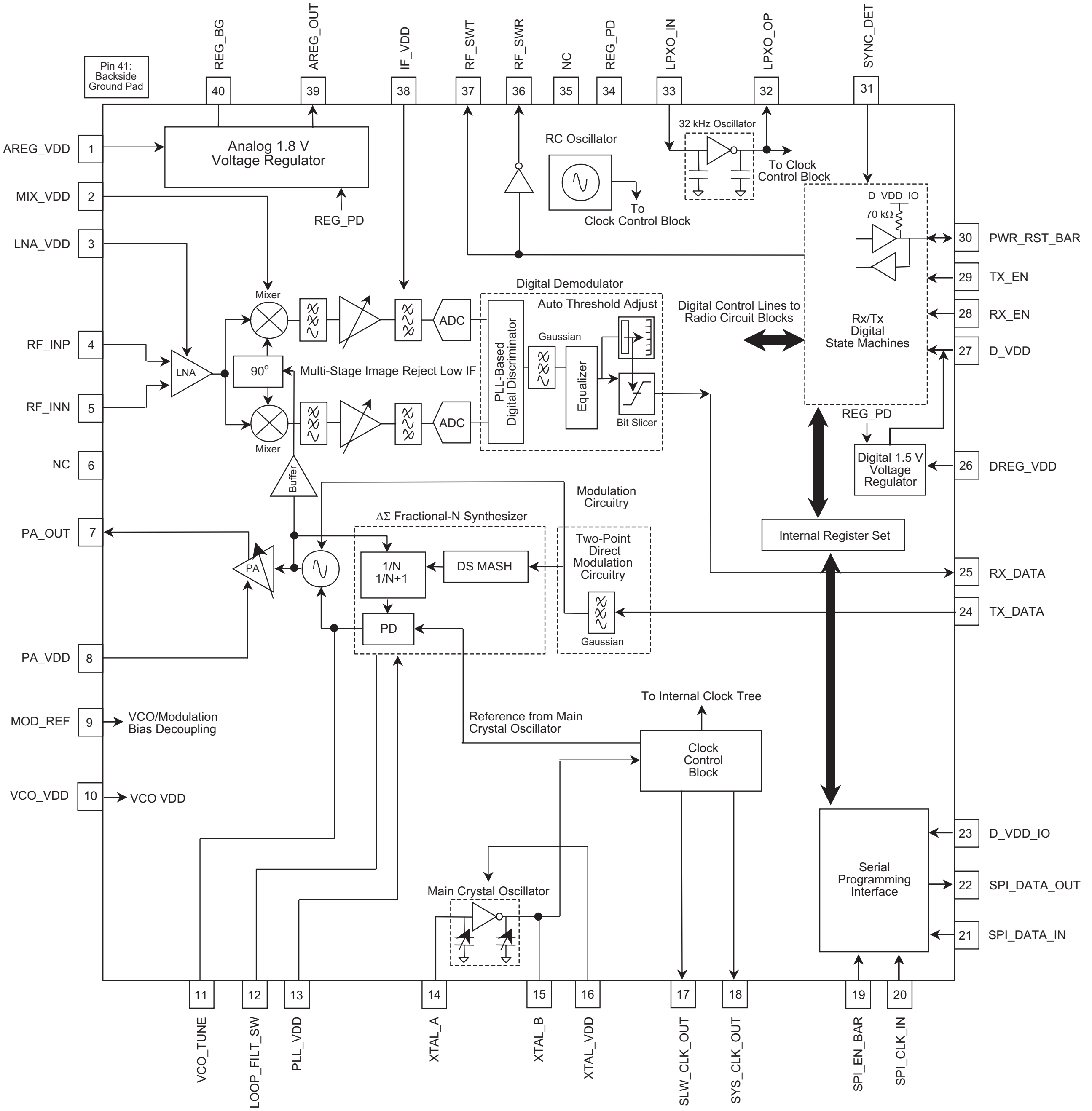


Figure 1 - XE1413 Block Diagram, in TQFN40 package top-view

2 PIN DESCRIPTION

Pin #	Name	Input/ Output (Note 1)	Digital/ Analog (Note 2)	Description
1	AREG_VDD	P	–	Input voltage to internal analog regulator (output 1.8V at pin 39)
2	MIX_VDD	P	–	Positive supply for the RF front end
3	LNA_VDD	P	–	Positive supply for the RF front end
4	RF_INP	I	A	Return path for RF input
5	RF_INN	I	A	RF input
6	NC	–	–	Do not connect
7	PA_OUT	O	A	Transmit PA output
8	PA_VDD	P	–	Positive supply for transmit PA
9	MOD_REF	O	A	VCO bias decoupling point
10	VCO_VDD	P	–	Positive supply for VCO
11	VCO_TUNE	I	A	VCO tuning port
12	LOOP_FILT_SW	O	A	Loop filter control
13	PLL_VDD	P	–	Positive supply for PLL
14	XTAL_A	I	A	Crystal oscillator input (MXTAL)
15	XTAL_B	O	A	Crystal oscillator output (MXTAL)
16	XTAL_VDD	P	–	Positive crystal oscillator supply
17	SLW_CLK_OUT	O	D	Slow digital clock output port
18	SYS_CLK_OUT	O	D	System digital clock output port
19	SPI_EN_BAR	I	D	SPI enable, active low
20	SPI_CLK_IN	I	D	SPI clock input port
21	SPI_DATA_IN	I	D	SPI data input port
22	SPI_DATA_OUT	O	D	SPI data output port
23	D_VDD_IO	P	–	Positive supply for the digital I/O pads
24	TX_DATA	I	D	Transmit data input port (from baseband)
25	RX_DATA	O	D	Over-sampled, bit sliced Rx data output to baseband
26	DREG_VDD	P	–	Input voltage to internal digital regulator (output 1.5V at D_VDD pin 27)
27	D_VDD	P	–	Positive supply voltage for digital circuits or regulated output of digital regulator
28	RX_EN	I	D	Receive sequence engaged when high (and TX_EN is low)
29	TX_EN	I	D	Transmit sequence engaged when high (and RX_EN is low)
30	PWR_RST_BAR	IO	D	Power-on reset and external reset. Bidirectional pin with open drain and internal 70 kΩ pull-up resistor to D_VDD_IO (pin 23)
31	SYNC_DET	I	D	Rx synchronization detect signal from baseband. If not used, connect a 100 kΩ resistor to D_VDD_IO (pin 23) or to ground and set register 0x1B, bit[7] = 0.
32	LPXO_OP	O	A	32 kHz low power crystal output. If not used, leave unconnected.
33	LPXO_IN	I	A	32 kHz low power crystal input. If not used, connect to ground.

Pin #	Name	Input/ Output (Note 1)	Digital/ Analog (Note 2)	Description
34	REG_PD	I	D	Regulator power-down pin for both regulators (D_VDD_IO = regulators disabled, Ground = regulators enabled)
35	NC	–	–	Do not connect
36	RF_SWR	O	D	RF switch output control port, active high during receive cycle (inverted RF_SWT signal). Pin 23 (D_VDD_IO) provides the “high” voltage for RF_SWR.
37	RF_SWT	O	D	RF switch output control port active high during transmit cycle (inverted RF_SWR signal). Pin 23 (D_VDD_IO) provides the “high” voltage for RF_SWT.
38	IF_VDD	P	–	Positive supply for IF analog circuitry
39	AREG_OUT	P	–	Regulated 1.8 V output from internal analog voltage regulator
40	REG_BG	–	–	Regulator Bang-Gap decoupling. Requires a 1 nF capacitor from pin 40 to ground when using internal 1.8 V regulator, AREG.
41	GND	G	–	Bottom ground pad.

Note 1: I = input, O = output, P = power, G = ground
Note 2: A = analog, D = digital

Table 1 - XE1413 Signal Descriptions

3 FUNCTIONAL DESCRIPTION

The XE1413 is an advanced, fully integrated mixed-signal digital radio transceiver specifically targeted for extreme low power Bluetooth applications. When combined with a low power baseband device (such as the Semtech SX1441, XE1431 or XE1402), the resulting solution consumes the lowest power of any other available Bluetooth system.

The following functional elements are integrated into the XE1413 device:

- Low noise Voltage Controlled Oscillator (VCO) with internal inductors and varactors
- Low noise fractional-N synthesizer
- Two point Gaussian Frequency Shift Keying (GFSK) modulator
- PA (Bluetooth Class 2 and 3 operation)
- Software adjustable transmit power control block (2 dB steps)
- Low-Noise Amplifier (LNA) and mixer
- High performance, dynamic Automatic Gain Control (AGC) system
- High performance, low Intermediate Frequency (IF) image reject filtering
- Dynamic “packet-by-packet” Received Signal Strength Indicator (RSSI) system
- Analog/Digital Converter (ADC), Phase Locked Loop (PLL)-based digital demodulator and bit slicer
- Low frequency, 32 kHz low power timing clock oscillator
- Two voltage regulators (1.8 V and 1.5 V)
- Transmit and receive timing control digital state machines
- Automatic synthesizer speed-up function
- Clock control block

3.1 RECEIVE BLOCK

The single-ended LNA is followed by a single stage In-Phase and Quadrature (I/Q) down conversion to a low IF. Effective image signal rejection is provided by IF signal processing in the complex signal domain, which allows the desired signal to be separated from the undesired image signal.

Since primary Bluetooth applications are mobile in nature, there are packet-to-packet changes in signal path propagation. Therefore, the multi-stage IF includes a fast AGC that adjusts the individual gains of each IF amplifier section on a packet-by-packet basis. AGC setting is automatically optimized for each received packet using the internal RSSI system. The AGC setting is established at an early stage during packet reception and remains fixed for the remainder of the packet.

Post-IF processing occurs in the digital domain after conversions using a low bit count ADC. A PLL-based digital demodulator that consists of a Gaussian filter, equalizer, data bit slicer, and automatic threshold adjust (frequency offset correction) allows the receiver to accurately track received signals that have poor frequency stability (transmit carrier drift due to “dirty” transmitters). Asynchronous data is presented at pin 25 (RX_DATA) and is over-sampled 13 times. The receiver does not provide symbol timing information. A baseband device is required to manage the symbol timing recovery, to select which of the samples provides the best Bit Error Rate (BER).

To facilitate fast frequency hopping performance, the XE1413 uses a low spurious, ΔΣ fractional-N synthesizer with a low noise integrated VCO. This combination allows a very high comparison frequency that provides a wide loop bandwidth for fast frequency hopping.

Several additional functions are incorporated to ensure rapid frequency acquisition. The LOOP_FILT_SW signal (pin 12) is used to dynamically switch to a lower loop filter resistor, which increases the loop bandwidth and effectively lowers the acquisition time. Charge pump current is also increased during acquisition. These functions are fully automatic and no baseband intervention is required.

3.2 TRANSMIT BLOCK

The fractional-N synthesizer enables a “no-IF” transmitter. The 2.4 GHz VCO is directly modulated by application of a two point filtered GFSK modulation approach. This eliminates the lower frequency oscillator, transmit IF, and transmit upconverter (mixer) associated with conventional transmitter architectures.

The single-ended PA transmit power output is set through software register settings. The PA power control function (i.e., ramp up) is controlled by the transmit state machine. As with all PAs, an abrupt transmit power transition causes poor spectral performance. The on-board transmit state machine ensures adherence to the Bluetooth spectral requirements. Again, this is an automatic function and requires no baseband intervention.

Operational control of the XE1413 requires limited baseband signaling. This efficiency is afforded by the timing control digital state machines. These state machines, one for receive and one for transmit, manage time critical radio functions that free the baseband from having to perform these tasks.

For specifics of the Bluetooth protocol, refer to the latest Bluetooth System Specification available from the official Bluetooth website at http://www.bluetooth.com/.

3.3 ANALOG CIRCUIT DESCRIPTIONS

This section describes the analog signals and circuit blocks required for any application design using the XE1413 RF transceiver.

3.3.1 LNA and Mixer Signals

The RF_INP (pin 4) and RF_INN (pin 5) signals provide the unbalanced input to the LNA. The MIX_VDD (pin 2) and LNA_VDD (pin 3) signals are dedicated power supply pins to the LNA and mixer blocks. The package ground pad provides the supply return path. Ensure that this pad is properly grounded to the PCB.

3.3.2 Differential PA Outputs

The PA_OUT signal (pin 7) is the single-ended output of the transmitter PA. Transmit power can be adjusted in 2 dB steps using the reg_tx_power register (0x01, bits [3:0]).

3.3.3 RF Analog Power Supplies

The PA_VDD (pin 8), VCO_VDD (pin 10), and IF_VDD (pin 38) signals are dedicated RF analog power supplies for the PA, VCO, and IF circuit blocks, respectively.

3.3.4 VCO Bias Decoupling Point

The MOD_REF (pin 9) signal is a VCO bias decoupling point that must be connected to ground with a capacitor.

3.3.5 PLL Loop Filter

The VCO_TUNE (pin 11), LOOP_FILT_SW (pin 12), and PLL_VDD (pin 13) signals connect to the on-board VCO and fractional-N PLL frequency synthesizer. The external PLL charge pump loop filter components connect from pin 11 (VCO_TUNE) to pin 13 (PLL_VDD).

Pin 12 (LOOP_FILT_SW) connects a second low value resistor in parallel with the primary loop filter resistor to improve settling times when a frequency hop takes place. This speed-up function is automatically controlled by the internal receive and transmit state machines.

3.4 MAIN CRYSTAL OSCILLATOR (MXTAL) BLOCK

A 13 MHz crystal connects to the XTAL_A (pin 14) and XTAL_B (pin 15) signals as illustrated in Figure 2 to complete the main crystal oscillator (MXTAL) circuit block. Register controlled, frequency adjust loading capacitors can be programmed using the reg_clock1 register (0x05, bits[3:0]). This feature allows the baseband to correct temperature-induced frequency drift.

When an external 13 MHz reference source is provided to the XE1413, place an AC coupling capacitor between the source and pin 15 (XTAL_B), and disconnect pin 14 (XTAL_A). Note that XTAL_VDD (pin 16) must be applied even when using an external reference signal source.

When an external reference is used, ensure that a clean, low phase noise, stable signal is presented to the XE1413. Use of buffers on the reference path should be used with caution as some low cost buffers may degrade performance.

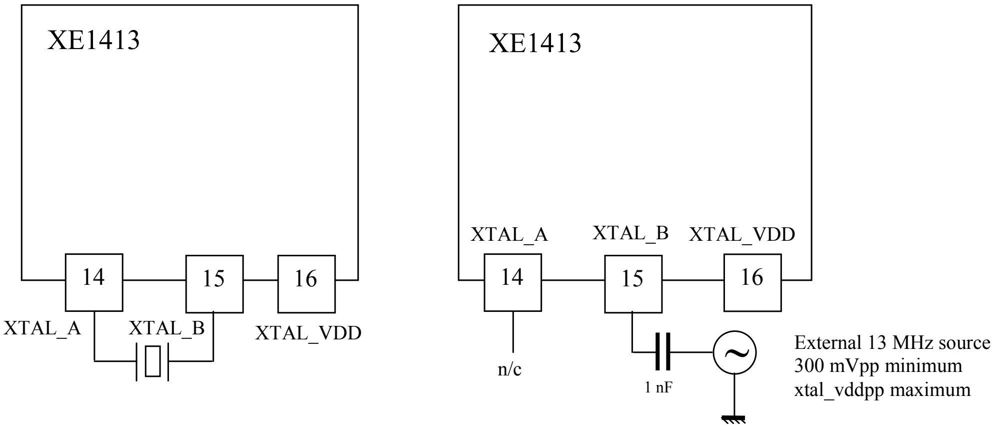


Figure 2 - Main Crystal Oscillator Diagram, with XTAL and external source respectively

3.5 LOW POWER CRYSTAL OSCILLATOR (LPXO) BLOCK

The low power crystal oscillator (LPXO) clock is not used or required by the XE1413 circuitry. This cost-saving feature is provided for baseband timing/clocking. It eliminates the need for a timing clock elsewhere in the system. Several clock signals are available from the XE1413 through pins 18 (SYS_CLK_OUT) and 17 (SLW_CLK_OUT). (Refer to the baseband interface description in this document.)

If an external 32 kHz crystal is not used, pin 32 (LPXO_OP) stays unconnected and pin 33 (LPXO_IN) should be connected to ground. The low power crystal oscillator should be placed in power-down mode using the reg_clock4 register (0x21, bit[7] = 1).

In the event that a 32 kHz clock is available from the system, it can be used to drive the LPXO_OP signal (pin 32). In this way the SYS_CLK_OUT signal (pin 18) can be used to provide either a 32 kHz or 13 MHz clock to the baseband device.

Caution must be exercised when driving the low power crystal oscillator from an external source. Radio performance should be verified in all operational states when using an external LPXO signal source (see Figure 3).

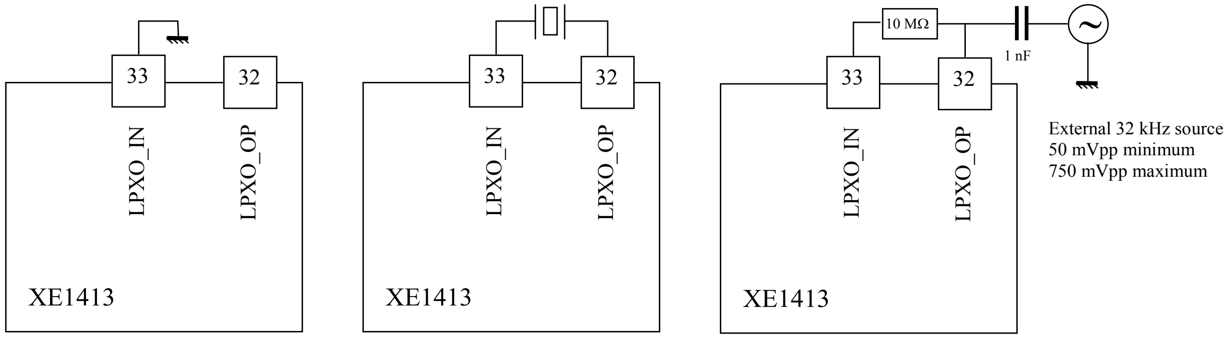


Figure 3 - LPXO External Source with configurations respectively: not used, 32KHz quartz, external source

3.6 INTERNAL VOLTAGE REGULATOR AND POWER PIN CONSIDERATIONS

The XE1413 offers two on-chip voltage regulators that eliminate external power supply components. One regulator (AREG) is intended to power the analog radio circuits while the other regulator (DREG) is for the digital circuits.

Current consumption is 25 µA for each regulator. It is recommended that both regulators are powered down whenever the XE1413 is in a power-down state. When the regulators are powered down, they enter a series pass mode in which they pass the unregulated voltage to the output.

Pin 34 (REG_PD) is the regulator power-down pin. The regulators are powered down when REG_PD equals D_VDD_IO. The regulators can also be powered down using register control.

3.6.1 Configuration Using Neither of the Two Internal Voltage Regulators.

The schematic diagram shown in Figure 4 indicates the power pin connections for those applications not using either of the internal voltage regulators. The REG_PD signal (pin 34) must be asserted high for this configuration.

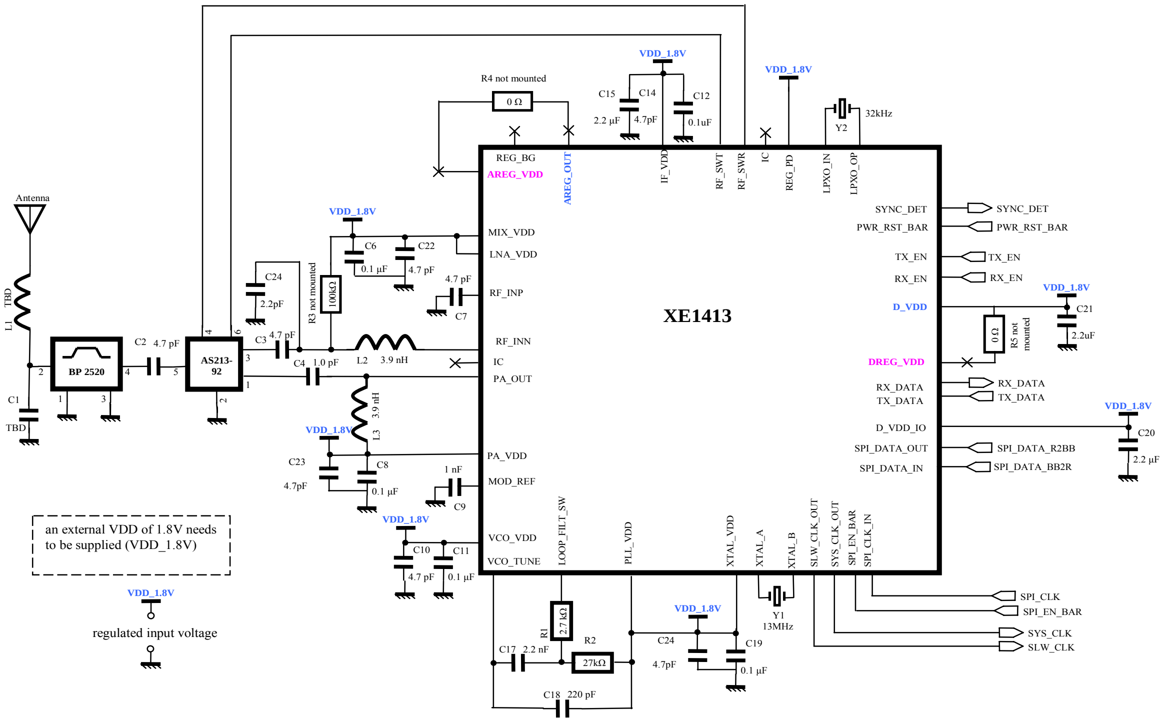


Figure 4 - Application diagram when voltage regulators are not used

3.6.2 Configuration Using Both Internal Regulators AREG and DREG

The schematic diagram shown in Figure 5 illustrates a typical circuit configuration using both internal regulators, AREG and DREG.

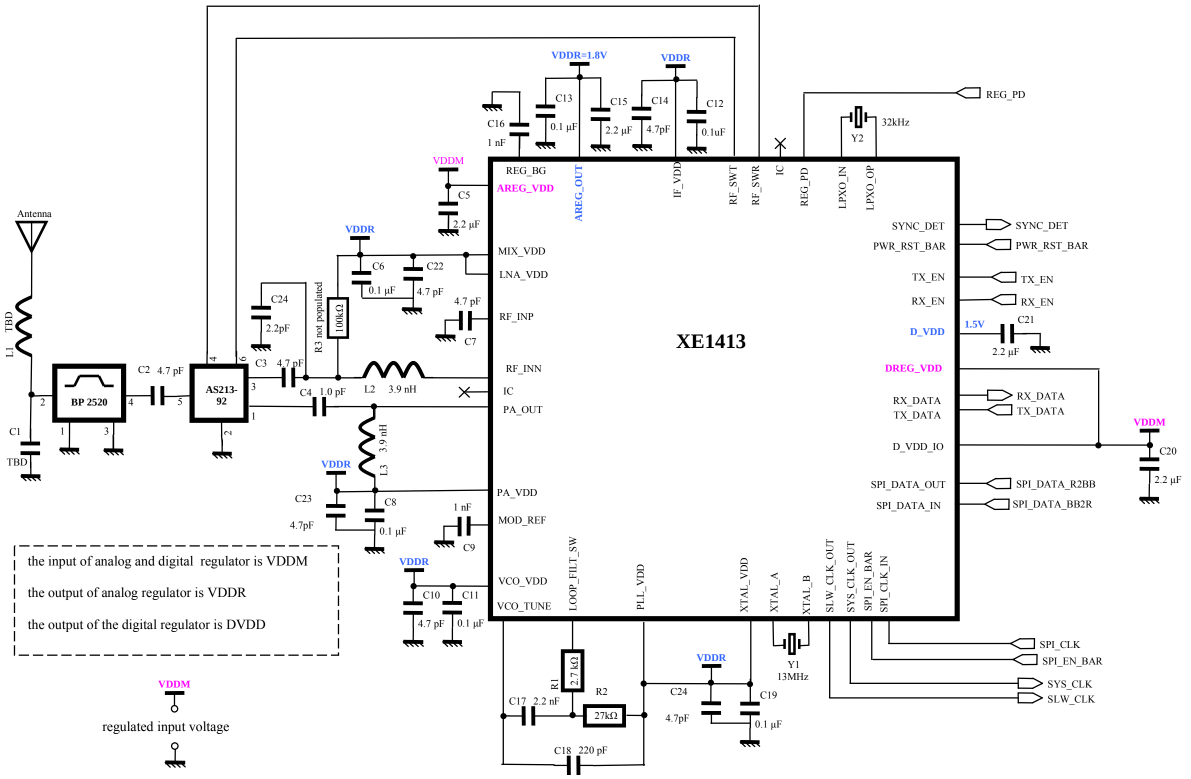


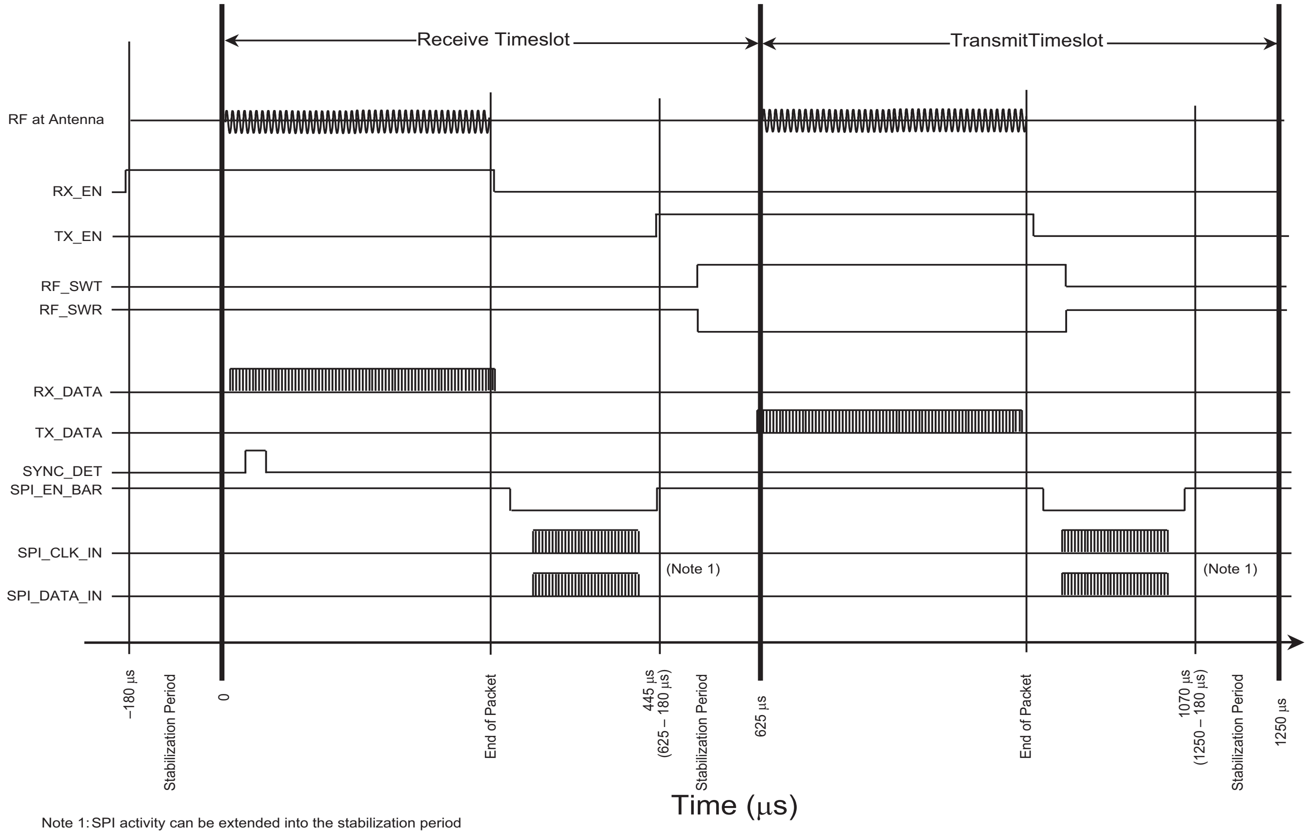
Figure 5 - Both Analog (1.8 V AREG) and Digital (1.5 V DREG) Voltage Regulators Operating

3.7 DIGITAL CIRCUIT DESCRIPTION

This section describes the digital signals and circuit blocks required for any application design using the XE1413 RF transceiver. Figure 6 presents the relationship between the baseband to XE1413 signaling and the air interface for a Bluetooth exchange. These timing sequences are explored in detail in this section and are for information only.

3.7.1 Timing Control Digital State Machines

The XE1413 timing control digital state machines manage the internal timing. One transmit and one receive state machine control the state of all internal circuit blocks. Internal timer settings have been optimized for peak radio performance. The only timing managed by the baseband device relates to the transmit and receive enable signals (TX_EN and RX_EN), and the transmit and receive data signals (TX_DATA and RX_DATA), in addition to tracking transmit and receive timeslots.



Note 1: SPI activity can be extended into the stabilization period but should be completed by the start of the next timeslot.

Figure 6 - Air Interface Timing

3.7.2 Transmit Timing State Machine Sequence

Figure 7 shows timing administered by the transmit state machine. A brief 6 μs warm-up time is activated on the rising edge of TX_EN, which is a general all-circuit stabilization period. All other activation sequence timings are referenced to the end of this 6 μs interval.

The circuit that requires the longest time to settle is the VCO/PLL. This circuit starts its frequency hop and phase settling as soon as the 6 μs warm-up time ends. Two techniques are applied to achieve rapid frequency hopping, increased charge pump current and decreased loop filter resistance. Both techniques increase the loop bandwidth offering a turbo, fast frequency switching mode.

The transmit/receive switch is engaged in the transmit state (RF_SWT, pin 37, goes high and RF_SWR, pin 36, goes low) 32 μs into the VCO/PLL settling period. This is followed 16 μs later by the PA turn-on/ramp-up. After 75 μs the PLL circuit switches from turbo to normal mode. The charge pump current is returned to the normal level and the low value loop filter resistor connected to LOOP_FILT_SW (pin 12) is switched out of the loop filter.

The VCO/PLL continues to settle until the 155 μs point (not shown in Figure 7). The final event is the application of modulation data to the transmitter at pin 24 (TX_DATA). This occurs at the 174 μs point after the 6 μs warm-up time.

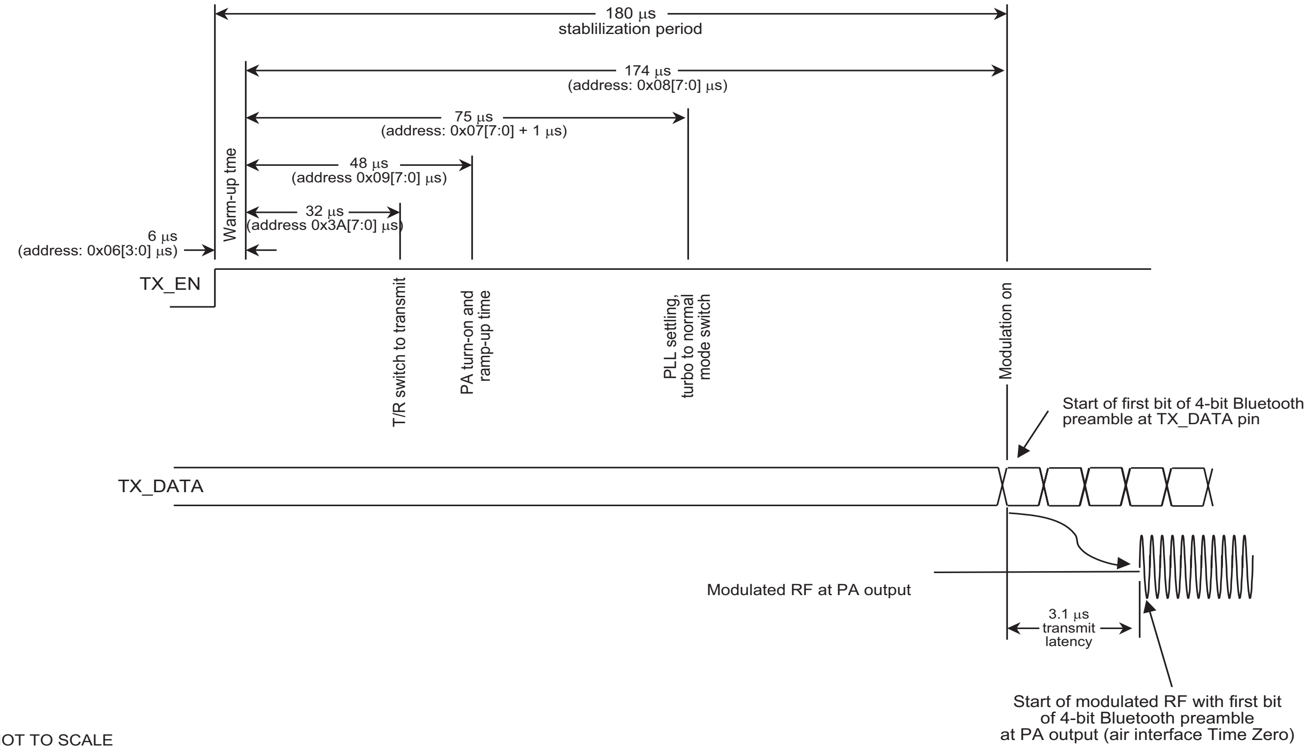
This effectively allows a guard time of 20 μs between VCO/PLL settling and modulation data application. Before the “Modulation On” instant, data present at TX_DATA is ignored by the XE1413.

The baseband must deliver the first transmit bit so that it appears at TX_DATA 180 μs after TX_EN is asserted high. The transmit state machine generates an internal 1 MHz clock used to sample TX_DATA. This internal clock is synchronized with the rising edge of TX_EN. The first sample occurs at the 180.5 μs point (0.5 μs after

"Modulation On"). Transmit data bits are sampled mid symbol provided that the data bit stream transitions occur at *x* µs (*x* integer) intervals from the rising edge of TX_EN.

The modulated carrier appears at the PA output 3.1 µs after the TX_DATA modulation begins (or more accurately, 3.1 µs after "Modulation On"). This delay – TX_DATA input to PA output – is known as the transmitter latency.

The activation sequence of the radio blocks as controlled by the state machine requires that the baseband assert the TX_EN signal 183.1 µs before the beginning of the active timeslot (air interface Time Zero). Therefore, the baseband must track when its next active timeslot is going to occur and then assert the TX_EN signal 183.1 µs before this event. This is followed 180 µs later by TX_DATA (3.1 µs before the timeslot begins). The Bluetooth specification allows a maximum timeslot window error of ±10 µs.



NOT TO SCALE

Figure 7 - XE1413 Transmit Timing Sequence

3.7.3 Receive Timing State Machine Sequence and the Synchronization Detect Function

The XE1413 features a synchronization detect function. This signal, input from the baseband, is used by the receive timing state machine to enhance the radio operation during the initiation of a Bluetooth session where the air interface timing is not yet known. Figure 8 shows the receive timing administered by the receive timing state machine. The warm-up time and VCO/PLL settling times are identical to the transmit timing sequence shown in Figure 7.

The receive circuits are activated in sequence (front-end, IF, demodulator). This power-up sequence completes in 8 µs.

Towards the end of the stabilization period, the RSSI system is enabled to monitor the incoming RF power level. The receive latency, the time between the beginning of a bit at the RF LNA input and the beginning of the demodulated bit at RX_DATA output, is shown to be 4.6 µs. Ideally, the baseband must assert RX_EN at least 182.4 µs before the beginning of the expected receive timeslot (air interface Time Zero). When a Bluetooth system is first activated it must find the piconet synchronization (timeslot boundaries), assuming an active piconet is in the vicinity. Once radio power-up sequences and initialization programming are complete, the baseband asserts the RX_EN signal (pin 28). Some time later (11 µs before the end of the stabilization period), the RSSI system begins to actively monitor the incoming RF power level (the IF amplifier gains are at maximum with the AGC operating in fast mode). This RF power detector is armed to trigger when the RSSI exceeds a threshold value. Whether this RF power is from a transmitting Bluetooth device, excess environmental noise, splatter from an adjacent channel, or some other source is unknown to the radio.

If the RF source is sufficiently high to be detected by the RSSI power detector, the radio becomes fully active. Active in this case means two events will occur:

1. RSSI information is used by the receive state machine to dynamically adjust the individual IF stage gains to optimize signal reception (with fast AGC mode)
2. RX_DATA output is enabled to output demodulated data (or noise, if no signal is present)

The receiver continues to operate under fast AGC and the IF stage gains are dynamically adjusted based upon the instantaneous RSSI level. This dynamic IF gain-adjust state exists until 30 µs beyond the end of the stabilization time. At that instant, the receive state machine begins to clamp the IF amplifier gains, stage by stage, and switches to slow AGC mode while continuing to output demodulated data on pin 25 (RX_DATA).

What happens after this point depends on whether the baseband has detected and recognized the access code.

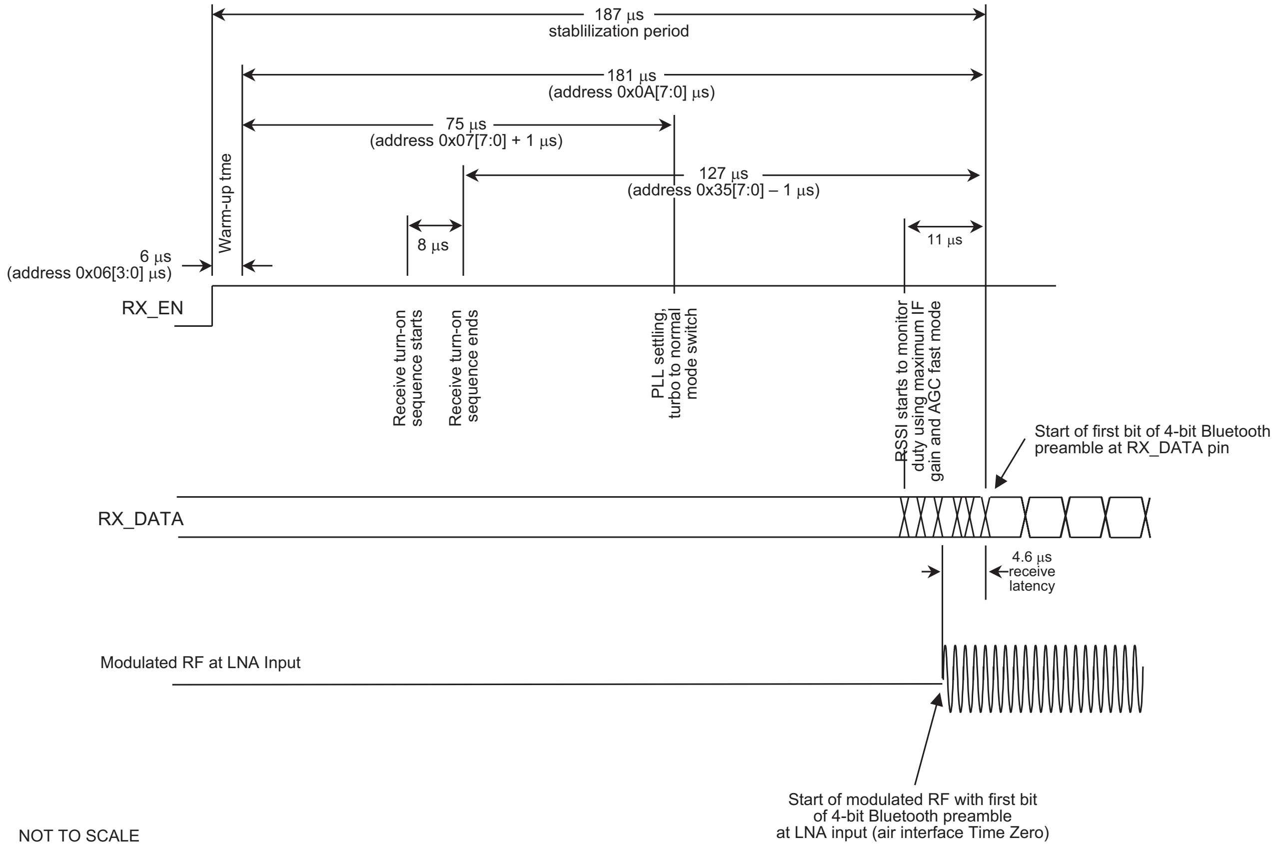


Figure 8 - XE1413 Receive Timing Sequence

1 **Baseband Detects and Recognizes the Access Code.** The receiver state machine locks the IF amplifier gain levels and switches to slow attack AGC mode. As long as the baseband asserts the SYNC_DETECT (pin 31) signal to the radio within 255 µs after the RF power detector has been triggered, the radio continues to demodulate the signal using slow AGC and current IF gain settings for the remainder of the packet. At the end of the packet, the baseband sets RX_EN low, de-activating the receiver.

2 **Baseband Cannot Recognize the Access Code.** Either the access code is not the desired one, or there is no transmitted signal at this instant. In either case, the radio continues to receive until 255 µs after the RF power detector has been triggered, at which point a time-out occurs.

The receive timing state machine monitors the SYNC_DETECT pin for activity. When the baseband does not recognize the access code, SYNC_DETECT is not asserted. The lack of this event causes the state machine to unfreeze the IF gains, switch to fast AGC mode, and re-arm the RSSI system RF power detector. All this occurs at the 255 μs point. If the RF power detector is triggered, the radio is activated and the process begins again.

In the event that the received RF energy is not sufficiently high to be detected by the RSSI RF power detector, the RSSI continues to monitor signal levels with maximum IF amplifier gains and fast AGC, but RX_DATA output is disabled. This state exists as long as RF power is not detected or until RX_EN is brought low by the baseband. Under ideal conditions, with only thermal noise at the antenna and RX_EN asserted, the RX_DATA output is inactive, IF gain is maximized, and AGC is in fast mode. The RX_DATA signal stays high or low and does not change state. The RSSI system threshold is set far below the Bluetooth sensitivity specification, which provides good receive sensitivity.

Best performance is achieved when using the synchronization detect function. If the baseband device does not support this operation, two alternative configurations may be used.

The first is to disable synchronization detect using the reg_sync_detect register (0x1B, bit[7] = 0) and tie the SYNC_DETECT pin to ground or to the D_VDD_IO pin.

The second alternative is to leave the synchronization detect function enabled and tie the SYNC_DETECT pin to the D_VDD_IO pin with a 100 kΩ pull-up resistor.

The power-up default state for the synchronization detect function is enabled.

3.8 BASEBAND INTERFACING AND SYMBOL TIMING RECOVERY

The XE1413 baseband interface provides fast, efficient baseband-radio interoperation. This section describes interface Symbol Timing Recovery (STR) and the related interface signals (TX_EN, RX_EN, and SYNC_DETECT are described elsewhere in this document). This interface is shown in Figure 9.

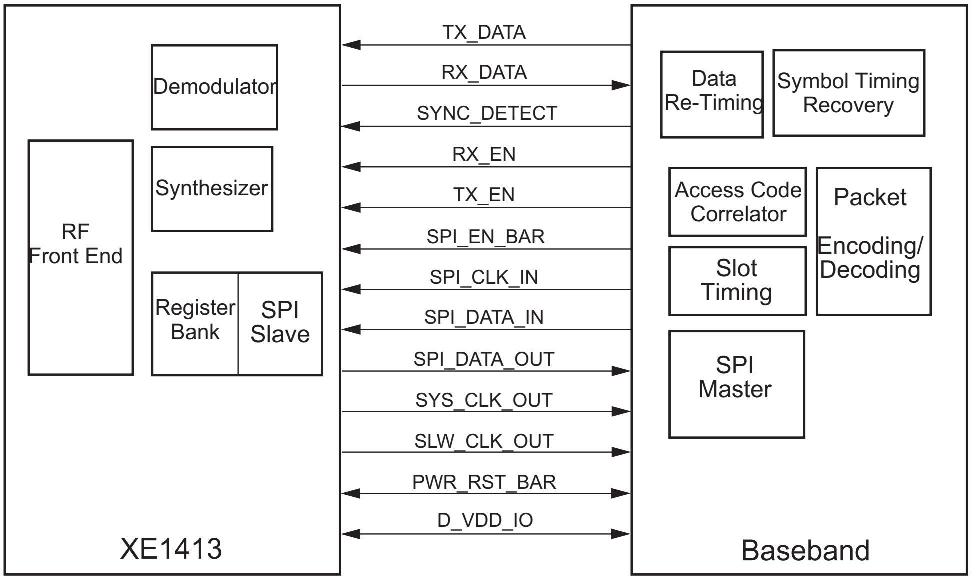


Figure 9 - XE1413 Baseband Interface

3.8.1 Baseband Symbol Recovery

The algorithm implemented inside the baseband system affects the STR, symbol recovery, and the BER sensitivity of the radio. The receive data appearing at the RX_DATA pin is a bit sliced demodulated output, presented without timing information.

Each receive data bit is composed of 13 digital samples. Under ideal, large SNR conditions, all 13 bit slices are the same level (either 1 or 0) and the data is clearly discernable to the eye when viewed on an analyzer. Symbol timing recovery under these conditions is a trivial exercise for the baseband. However, with non-ideal conditions (low SNR), each data bit received appears at the RX_DATA pin with some of the 13 samples dropped out (i.e., if the transmitted data bit is a 1, not all of the 13 samples would be set to 1). This causes a level of uncertainty concerning the location of the bit cell boundaries (symbol timing) and, to a lesser extent, the data bit value (whether 1 or 0). The analyzer display would appear with 'noisy' or 'jittered' bit cell boundaries, complicating STR determination. The internal filtering prevents dropouts from occurring mid-symbol.

As the SNR continues to decrease, the number of ‘noisy’ samples encroaches upon the middle of the symbol.

Various techniques and approaches may be applied by a particular baseband. In all cases, the solution requires two determinations:

1. Establish the STR (i.e., determine where the bit cell boundaries occur)
2. Apply decision criteria to discern a 1 or 0

The most common STR approaches are over-sampling with correlation (applied to the access code word) and PLL transition tracking. The decision criteria are also subject to differing approaches.

The use of a correlator STR scheme is strongly recommended. It will offer the best radio sensitivity and Carrier-to-Interference (C/I) performance.

A poorly designed STR and decision criteria mechanism can degrade radio BER sensitivity performance. As such, an awareness of the particular baseband algorithm is desirable. A baseband that applies over-sampling with majority vote decision criteria using all samples causes a degraded BER since the samples near the edge of the symbol boundaries have a high probability of error that can negatively influence the decision error probability.

The best approach is to use over-sampling to identify symbol timing only. To determine the bit value, use the one sample that lies midway between bit cell boundaries. Do not use a majority vote decision criteria.

Note that some basebands may only perform STR at the beginning of the packet. Therefore, if the transmitting system's crystal oscillator (reference source) and/or the receiving baseband crystal oscillator differ significantly from their nominal frequencies, the BER can degrade towards the end of a packet.

This problem may manifest itself as high BER on DH3 or DH5 packets, but acceptable BER on DH1 packets. As long as the transmitting and receiving reference sources meet the Bluetooth requirement for frequency accuracy (< ±20 ppm), no BER degradation occurs over the longest Bluetooth packet (DH5).

For example, assume the receiver reference source is at +20 ppm while the transmitter reference source is at –20 ppm. The total difference is 40 ppm. Over a DH5 packet (i.e., 3000 symbols), the drift at the end of the packet would be:

$$3000\ \mu s \times 40 \cdot 10^{-6}\ ppm = 120\ ns$$

With the XE1413 internal over-sampling at 13 MHz (every 77 ns), this error does not encroach upon the middle of the symbol, so BER performance is not degraded.

Baseband sampling of the RX_DATA pin should be synchronized with the radio’s 13 MHz clock (SYS_CLK_OUT, pin 18) for best performance. The RX_DATA output transitions on the rising edge of SYS_CLK_OUT.

3.9 CLOCK CONTROL BLOCK AND OSCILLATOR CONTROL

As illustrated in Figure 10, this block provides control of all oscillator/clock functions on the XE1413. There are three oscillators (RC, MXTAL and LXPO) as inputs to the clock control block and two output clock pins on the XE1413. These output clock pins (SYS_CLK_OUT and SLW_CLK_OUT) are used to provide clock signals to the baseband device. The SLW_CLK_OUT and SYS_CLK_OUT signals can be enabled or disabled if the application does not require them.

Figure 10 shows the different possible routing options, settings of multiplexers and the corresponding SPI registers.

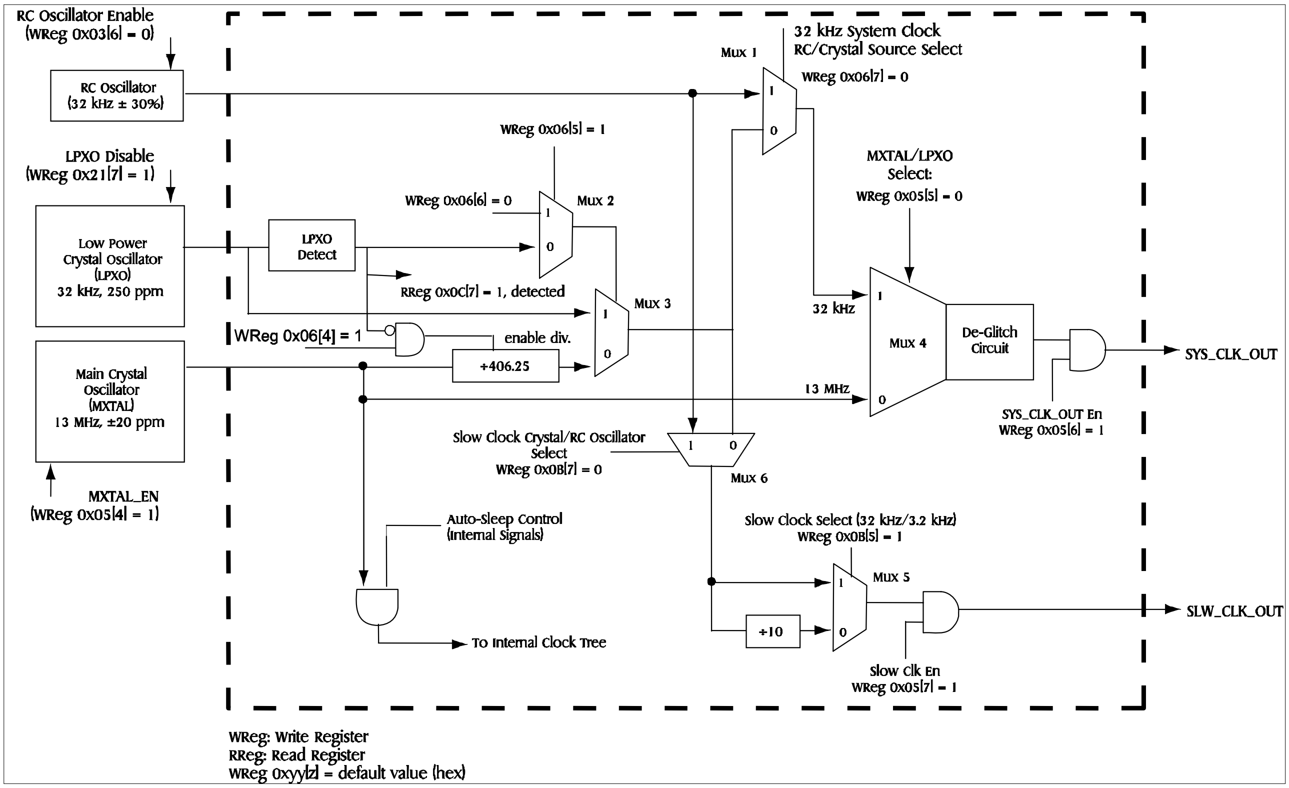


Figure 10 - Clock Control Block

3.9.1 Main Crystal Oscillator (MXTAL)

This oscillator provides a 13 MHz clock to the clock control block and can be routed only to the SYS_CLK_OUT. Alternatively, the 13 MHz clock can be divided and then be provided as a slow clock at SYS_CLK_OUT (32 kHz) or SLW_CLK_OUT (3.2 kHz or 32 kHz) This slow clock is generated by the 1/406.25 divider. In the 3.2 kHz case, a further 1/10 division can be applied.

MXTAL can be powered down in the case a 13 MHz clock is not required (standby modes). Once MXTAL is powered down an automatic MXTAL start-up function is armed (this function is described elsewhere in this document). Start up time for MXTAL is 8 to 10 ms.

3.9.2 Low Power Crystal Oscillator (LPXO)

The output of this oscillator can be routed to either SYS_CLK_OUT (at 32 kHz) or SLW_CLK_OUT (3.2 kHz or 32 kHz), The LPXO clock is not required by the XE1413 for its own operation and can be suppressed if the application does not require a low frequency clock.

An automatic LPXO detect circuit is incorporated into the clock control block to detect the presence of the 32 kHz signal from LPXO. When this circuit is enabled the LPXO oscillation signal, if present, causes the LPXO detect output to go high.

When no 32 kHz signal is detected by the LPXO detect circuit the derived 32 kHz clock from the 13 MHz MXTAL will be selected.

When there is no LPXO crystal installed or there is no external 32 kHz clock driving the LPXO buffer, the buffer should be configured in power-down mode.

3.9.3 RC Oscillator

This oscillator provides a very low power (<10 μA), 32 kHz ± 30% clock. The RC oscillator can be output to SYS_CLK_OUT or SLW_CLK_OUT. The RC oscillator also plays a role in the power-on reset function of the XE1413.

- SYS_CLK_OUT: Mux 1, using the reg_clock2 register (0x06, bit[7] = 1), and Mux 4, using the reg_clock1 register (0x05, bit[5] = 1)
- SLW_CLK_OUT: Mux 6 and Mux 5

The RC oscillator also plays a role in the power-on reset function of the XE1413. The SLW_CLK_OUT and SYS_CLK_OUT signals are enabled using the reg_clock1 register (0x05, bit[7] = 1 and bit[6] = 1, respectively).

3.9.4 SLW_CLK_OUT State During Active Rx and Tx Periods

The SLW_CLK_OUT signal should be disabled during the active period of receive and transmit timeslots by setting bit[7] = 0 in the reg_clock1 register (0x05). Failure to do so may degrade radio performance.

3.9.5 Auto-Sleep Function

An auto-sleep function gates the 13 MHz clock to the XE1413 radio blocks and powers them down. This feature ensures the lowest inter-packet current consumption. The oscillators (MXTAL, LPXO, and RC), clock control block, and SYS_CLK_OUT and SLW_CLK_OUT pins are independent of the auto-sleep function.

3.9.6 32 kHz/13 MHz SYS_CLK_OUT Clock Transition/De-Glitch Circuit

A de-glitch feature prevents extraneous clock edges when switching between 32 kHz and 13 MHz outputs on the SYS_CLK_OUT pin (refer to Figure 11 and Figure 12 for the respective timing diagrams). The 16 ms delay shown in Figure 12 between the SPI_EN_BAR signal going low and the SYS_CLK_OUT signal switching to 13 MHz is due largely to MXTAL start-up time.

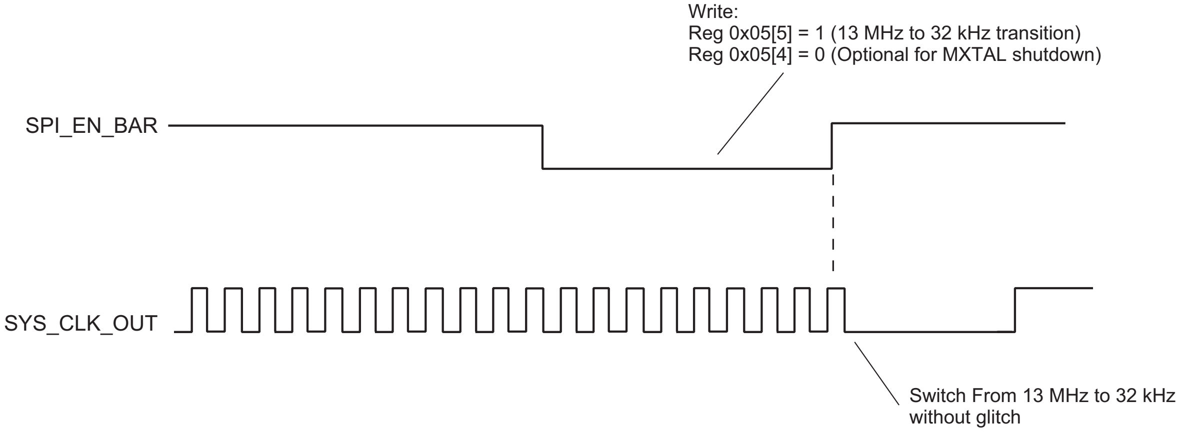


Figure 11 - Timing Diagram, 13 MHz to 32 kHz

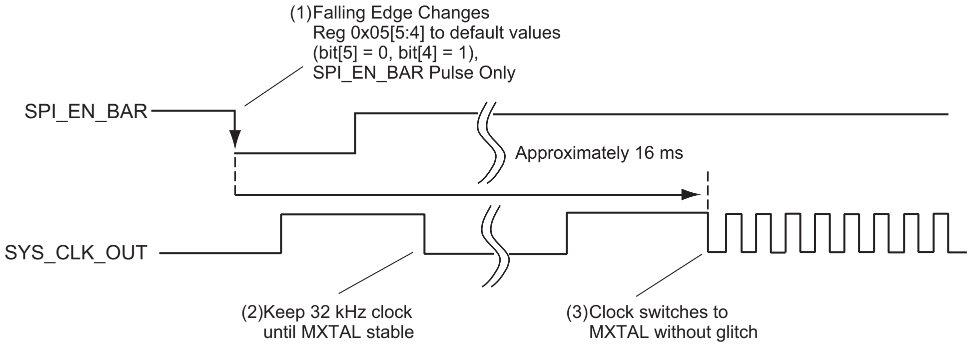


Figure 12 - Timing Diagram, 32 kHz to 13 MHz

3.9.7 Automatic MXTAL Start-up Function

An automatic MXTAL start-up function can be used to activate MXTAL when it has been disabled. This function operates in conjunction with the 32 kHz/13 MHz SYS_CLK_OUT transition/de-glitch feature.

Triggered into action by a falling edge on SPI_EN_BAR, this feature immediately sets bit[4] = 1 in the reg_clock1 register (0x05) to enable MXTAL. Once a start-up and stabilization period for MXTAL ends (approximately 16 ms), bit[5] in this register is set to 0 to transition SYS_CLK_OUT to 13 MHz from 32 kHz, glitch-free.

To use this feature, bits[5:4] in the reg_clock1 register (0x05) are set to 10b. At this point, the following states exist:

- A 32 kHz clock is present on SYS_CLK_OUT (transitioned from 13 MHz to 32 kHz without glitches using the transition/de-glitch circuit).
- All radio blocks are powered down.
- MXTAL is powered down.
- The RC oscillator may or may not be powered down depending on the state of bit[6] in the reg_rc_osc register (0x03). The default state is enabled (bit[6]=0)
- SLW_CLK_OUT may or may not be active depending on the state of bit[7] in the reg_clock1 register (0x05) and the 32 kHz source. The source of this 32 kHz clock is assumed to be the low power crystal oscillator, LPXO (alternative source is the RC oscillator, which must be selected by bit[7] in the reg_clock2 register, 0x06, before MXTAL is disabled).

The automatic MXTAL enable function relieves the baseband from having to enable MXTAL through register access, allowing it to immediately program the channel/power registers while MXTAL is starting up. Although nominal start-up time for MXTAL is 8 to 10 ms, a 16 ms start-up period ensures sufficient guard time.

Note that the last SPI activity must be to set bits[5:4] in the reg_clock1 register (0x05) to 10b, which powers down MXTAL and arms the automatic MXTAL start-up function.

3.9.8 Clock Control Default States

The clock control block diagram in Figure 10 shows the default power-on register configuration. This default state comprises the following conditions:

- MXTAL enabled: reg_clock1 register (0x05), bit[4] = 1
- RC oscillator enabled: reg_rc_osc register (0x03), bit[6] = 0
- LPXO disabled, reg_clock4 register (0x21), bit[7] = 1
- 13 MHz clock present on SYS_CLK_OUT (pin 18): reg_clock1 register (0x05), bit[5] = 0
- SLW_CLK_OUT (pin 17) is enabled
- LPXO auto detect is disabled: reg_clock2 register (0x06), bit[5] = 1

3.10 SERIAL PROGRAMMING INTERFACE (SPI)

The SPI enables the baseband to read/write non-time critical data to/from the XE1413. The SPI is a standard four-pin interface. Ideally, all SPI activity should take place during inter-packet intervals when both TX_EN and RX_EN signals are low. SPI activity during transmit or receive may interfere with radio performance. However, SPI activity can be extended into the stabilization period but should be completed by the start of the next timeslot (refer to Figure 6).

SPI_EN_BAR. This is an active low signal that activates the SPI interface. The baseband is expected to drive the SPI_EN_BAR signal low when it wants to communicate with the XE1413.

SPI_CLK_IN. This signal is the serial interface clock from the baseband device. The XE1413 samples the SPI data on the rising edge of the SPI_CLK_IN signal. The SPI_CLK_IN frequency can be between 1 and 5 MHz.

SPI_DATA_OUT. This signal is the data communication line from the XE1413 to the baseband device.

SPI_DATA_IN. This signal is the data communication line from the baseband device to the XE1413.

3.11 SERIAL WRITE OPERATION

SPI transfers are arranged in a multi-byte format with the minimum transfer being two bytes. The first byte consists of a one-bit read/write flag and a seven-bit address. The second byte is the data.

Data bytes from consecutive addresses can be written or read with the address auto-increment feature. This allows the entire register file contents to be read or written in a single operation by simply holding SPI_EN_BAR low for an extended period while continuing to apply the SPI_CLK_IN clock.

Refer to Figure 13 and Figure 14 for detailed SPI timing information.

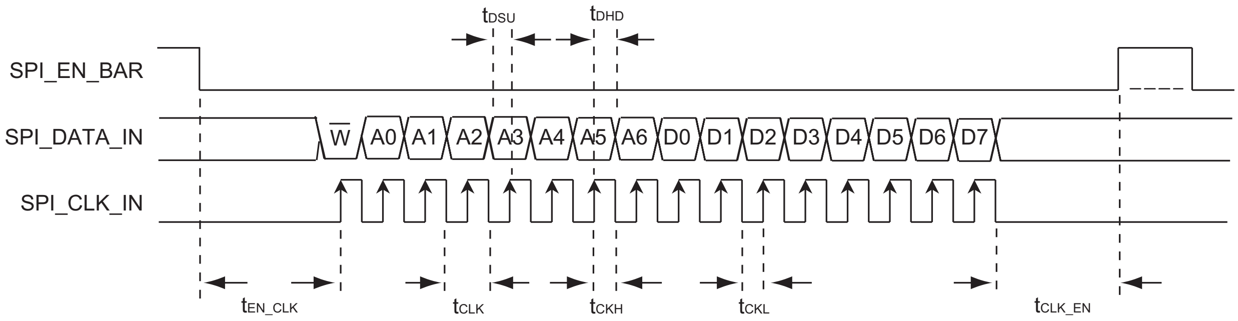


Figure 13 - Baseband Write to XE1413 Timing Diagram

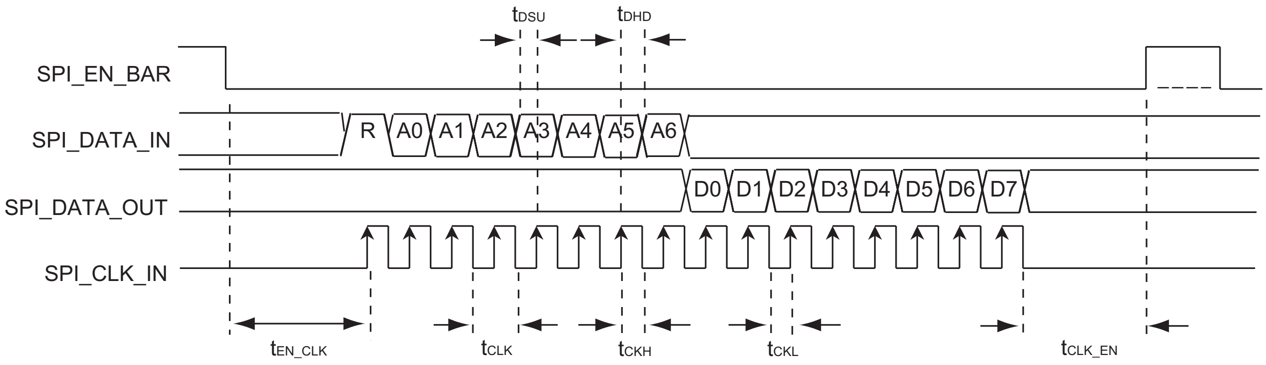


Figure 14 - Baseband Read From XE1413 Timing Diagram

3.12 RESET PIN OPERATION

The reset signal, PWR_RST_BAR (pin 30), is bi-directional. The output device of this pin uses an open drain configuration with an internal 70 kΩ pull up resistor to D_VDD_IO. Two reset functions exist:

- A power-on reset occurs when the supply voltage is applied to the device. The XE1413 drives PWR_RST_BAR low for 50 ms as timed by the internal RC oscillator. After this interval, the pin becomes an input and is pulled up to D_VDD_IO by the internal resistor. All register values are set to their default values listed elsewhere in this document (refer to Figure 15).
- A soft reset occurs when the baseband drives PWR_RST_BAR low for a minimum of 10 µs anytime after the power-on reset event. All registers are reset to their default values except for bits[5:4] in the reg_clock1 register at address 0x05.

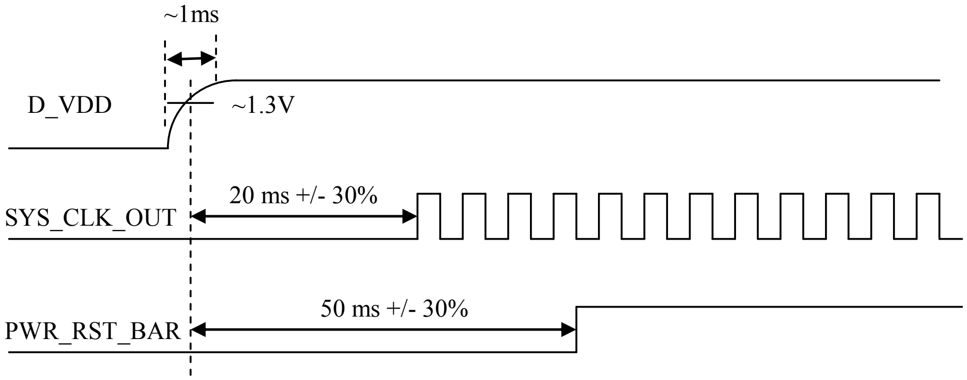


Figure 15 - Power-On Sequence with typical values

3.13 REGISTERS

User-programmable XE1413 registers are summarized in Table 2. Table 3 through to Table 15 provide more detailed descriptions of each register. By default, all registers are readable by the baseband controller.

Under normal operation, the only SPI traffic should be to the reg_channel register (0x00), reg_tx_power register (0x01), and reg_rssi register (0x02).

Do not access register addresses not listed in Table 2. Writing to these unlisted, reserved registers causes erroneous device operation. If during design testing, one of these registers is inadvertently modified, simply execute a reset using the PWR_RST_BAR pin.

All bits marked "Reserved" in Table 3 through Table 15 must not be changed. Caution must be exercised when the baseband is programming registers with reserved bits.

Address (Hexadecimal)	Register Name	W/R (Note 1)	Description
00	reg_channel	W	Channel frequency selection
01	reg_tx_power	W	Transmit power attenuation
02	reg_rssi	R	Receive Signal Strength Indicator (RSSI)
03	reg_rc_osc	W	RC oscillator enable
05	reg_clock1	W	Clock selection and crystal tuning
06	reg_clock2	W	Low frequency clock source select
0B	reg_clock3	W	Low frequency clock source select
0C	reg_sensors	R	Crystal detect
1B	reg_sync_detect	W	Synchronization detect enable
21	reg_clock4	W	Low power crystal oscillator enable
36	reg_sync_detect_timer	W	Maximum time from detected RF power to rising edge of SYNC_DET
3D	reg_chipcode	R	Device revision code
3F	reg_regulator_pwdn	W	Voltage regulator power-down control

Note 1: Reflects the direction of information flow between the baseband and the XE1413. W indicates that the contents of the register are expected to be written to by the baseband device. An R indicates that the baseband only reads information; an attempt to write has no effect on the operation of the XE1413.

Table 2 - XE1413 Register Summary

Bit Location	Description	Reset State (0x00)
7	Reserved (Note 1)	0
6:0	Channel frequency selection: 0x00 = 2.402 GHz 0x4E = 2.480 GHz	0000000

Note 1:"Reserved" bits must not be changed. This register sets the current channel in the synthesizer. Must be loaded before a rising edge on TX_EN or RX_EN.

Table 3 - reg_channel Register (0x00)

Bit Location	Description	Reset State (0x00)
7:4	Reserved (Note 1)	0000
3:0	Transmit power control in 1.8 ±0.4 dB steps: 0x00 = 0 dBm nominal 0x08 = –14 dBm nominal 0x0F = –27 dBm nominal	0000

Note 1: "Reserved" bits must not be changed.

Table 4 - reg_tx_power Register (0x01)

Bit Location	Description	Reset State (0xxx)
7	Reserved (Note 1)	0
6:0	RSSI digital readout for last received packet. Value in decimal represents signal level in dBm (e.g., 0x14 = –20 dBm; 0x32 = –50 dBm). The RSSI level is latched into register 0x02 approximately 30 µs after the start of the receive packet. The SPI should not access the XE1413 during an active transmit or receive session. Doing so may degrade the BER. The RSSI level is kept until the next receive slot.	xxx xxxx

Note 1: "Reserved" bits must not be changed.

Table 5 - reg_rssi Register (0x02)

Bit Location	Description	Reset State (0x12)
7	Reserved (Note 1)	0
6	RC oscillator enable: 0 = enable, 1 = disable	0
5:2	Reserved (Note 1)	0100
1	Reserved (Note 1)	1
0	Reserved (Note 1)	0

Note 1: "Reserved" bits must not be changed.

Table 6 - reg_rc_osc Register (0x03)

Bit Location	Description	Reset State (0xD8)
7	SLW_CLK_OUT enable: 1 = enable, 0 = disable	1
6	SYS_CLK_OUT enable: 1 = enable, 0 = disable	1
5 (Note 1)	SYS_CLK_OUT frequency selection: 1 = select 32 kHz output (from one of: RC oscillator, 32 kHz LPXO, or divided 13 MHz MXTAL). 0 = select 13 MHz output (from 13 MHz crystal oscillator)	0
4 (Note 1)	MXTAL oscillator enable: 1 = enabled, 0 = disabled	1

Bit Location	Description	Reset State (0xD8)
3:0	4-bit crystal oscillator (MXTAL) tuning. Assumes 10 pF loading capacitor, 13 MHz crystal. Due to internal loading capacitors, no external capacitors are required. 0000 = +36 ppm nominally (±20%) 1111 = –36 ppm nominally (±20%)	1000

Note 1: This bit is only reset when power is applied to the XE1413. The reset signal, PWR_RST_BAR, does not reset this bit.

Table 7 - reg_clock1 Register (0x05)

Bit Location	Description	Reset State (0x36)
7	RC oscillator/XTAL source for 32 kHz: 1 = RC oscillator, 0 = one of the crystal oscillators (either MXTAL or LPXO)	0
6	MXTAL/LXTAL 32 kHz SYS_CLK_OUT manual source selection (MXTAL or LPXO)	0
5	MXTAL/LXTAL 32 kHz auto/manual selection for 32 kHz SYS_CLK_OUT source	1
4	Reserved (Note 1)	1
3:0	Reserved (Note 1)	0110

Note 1: “Reserved” bits must not be changed.

Table 8 - reg_clock2 Register (0x06)

Bit Location	Description	Reset State (0x34)
7	SLW_CLK_OUT source: 1 = RC oscillator, 0 = either MXTAL or LPXO crystal oscillator	0
6	RC oscillator 128 kHz/32 kHz frequency select (1 = 128 kHz, 0 = 32 kHz)	0
5	SLW_CLK_OUT 32 kHz/3.2 kHz select (1 = 32 kHz, 0 = 3.2 kHz)	1
4:0	Reserved (Note 1)	10100

Note 1: “Reserved” bits must not be changed.

Table 9 - reg_clock3 Register (0x0B)

Bit Location	Description	Reset State (0x07)
7	LPXO oscillator detect: 0 = not detected,1 = detected	0
6:3	Reserved (Note 1)	0000
2	MXTAL oscillator detect: 1 = detected, 0 = not detected	1
1:0	Reserved (Note 1)	11

Note 1: “Reserved” bits must not be changed.

Table 10 - reg_sensors Register (0x0C)

Bit Location	Description	Reset State (0xFD)
7	Synchronization detect: 1 = enabled, 0 = disabled	1
6:0	Reserved (Note 1)	1111101

Note 1: “Reserved” bits must not be changed.

Table 11 - reg_sync_detect Register (0x1B)

Bit Location	Description	Reset State (0x84)
7	Low power LPXO crystal enable_bar: 0 = enabled, 1 = disabled	1
6:0	Reserved (Note 1)	0000100

Note 1: “Reserved” bits must not be changed.

Table 12 - reg_clock4 Register (0x21)

Bit Location	Description	Reset State (0xFF)
7:0	This value specifies the time, in µs, that the baseband IC has to return a synchronization detect signal to the XE1413 once its RF power detector has been triggered.	11111111

Table 13 - reg_sync_detect_timer Register (0x36)

Bit Location	Description	Reset State (0x72)
7:0	Chip revision code	01110010

Table 14 - reg_chipcode Register (0x3D)

Bit Location	Description	Reset State (0x00)
7	Digital regulator DREG power down: 0 = enable, 1 = power down	0
6	Analog regulator AREG power down: 0 = enable, 1 = power down	0
5:0	Reserved (Note 1)	000000

Note 1: “Reserved” bits must not be changed.

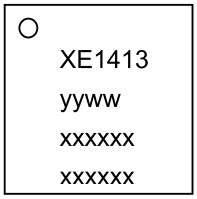
Table 15 - reg_regulator_pwdn Register (0x3F)

4 PACKAGE INFORMATION

Package dimensions (all in mm) for the XE1413 40-pin TQFN lead-free are shown below. The marking is shown in

top view

Figure 16:



top view

Figure 16 - XE1413 Marking

4.1 ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY

The XE1413 is a static-sensitive electronic device. Do not operate or store near strong electrostatic fields. Take proper ESD precautions.

4.2 SOLDERING REFLOW PROFILE

The soldering reflow profile used by XE1413 is described in the standard IPC/JEDEC J-STD-020C (see http://www.jedec.org/download/search/jstd020c.pdf).

4.3 ELECTRICAL AND MECHANICAL SPECIFICATIONS

The absolute maximum ratings of the XE1413 are provided in Table 16. The electrical specifications are provided in Table 17 and the state definitions are in Table 18.

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage to analog or digital circuits	VDD	–0.5	+3.6	V
I/O supply to baseband digital interface	VDD_{IO}	–0.5	+3.6	V
Voltage applied to any input	$V_{IN\_MAX\_ANALOG}$	–0.5	VDD	V
Voltage applied to any input	$V_{IN\_MAX\_DIGITAL}$	–0.5	VDD_{IO}	V
Storage temperature	$T_{STORAGE}$	–65	+125	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal values.

Table 16 - XE1413 Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
General Specifications						
Analog supply voltage	A_VDD	Pins 2, 3, 8, 10, 13, 16, and 38 only	1.7	1.8	2.2	V
Digital supply voltage (must be within ±0.3 V of analog supply voltage)	D_VDD	Pin 27 only	1.4	1.8	2.4	V
Digital I/O positive supply voltage (D_VDD_IO ≥ A_VDD – 0.3 V)	D_VDD_IO	Pin 23 only	1.5	1.8	3.6	V
Voltage regulator input voltage for 1.8 V regulator (AREG)	AREG_VDD	Pin 1 only	2.3	3.0	3.6	V
Voltage regulator input voltage for 1.5 V regulator (DREG)	DREG_VDD	Pin 26 only	2.3	3.0	3.6	V
Operating temperature range, Bluetooth-compliant	T_{OP}		–40		+85	°C
Digital DC Characteristics						
Logic high level in	V_{IN_HIGH}		VDD_{IO} – 0.4			V
Logic low level in	V_{IN_LOW}				0.4	V
Logic high level out	V_{OUT_HIGH}		VDD_{IO} – 0.4			V
Logic low level out	V_{OUT_LOW}				0.4	V
Logic high level out	I_{OUT_HIGH}		2			mA
Logic low level out	I_{OUT_LOW}		2			mA
Logic output load capacitance	C_{OUT}				10	pF
Logic input capacitance	C_{IN}				2	pF
Receive						
Operating frequency	f_{OP}		2.402		2.480	GHz
Channel spacing	f_{CHAN}			1.0		MHz

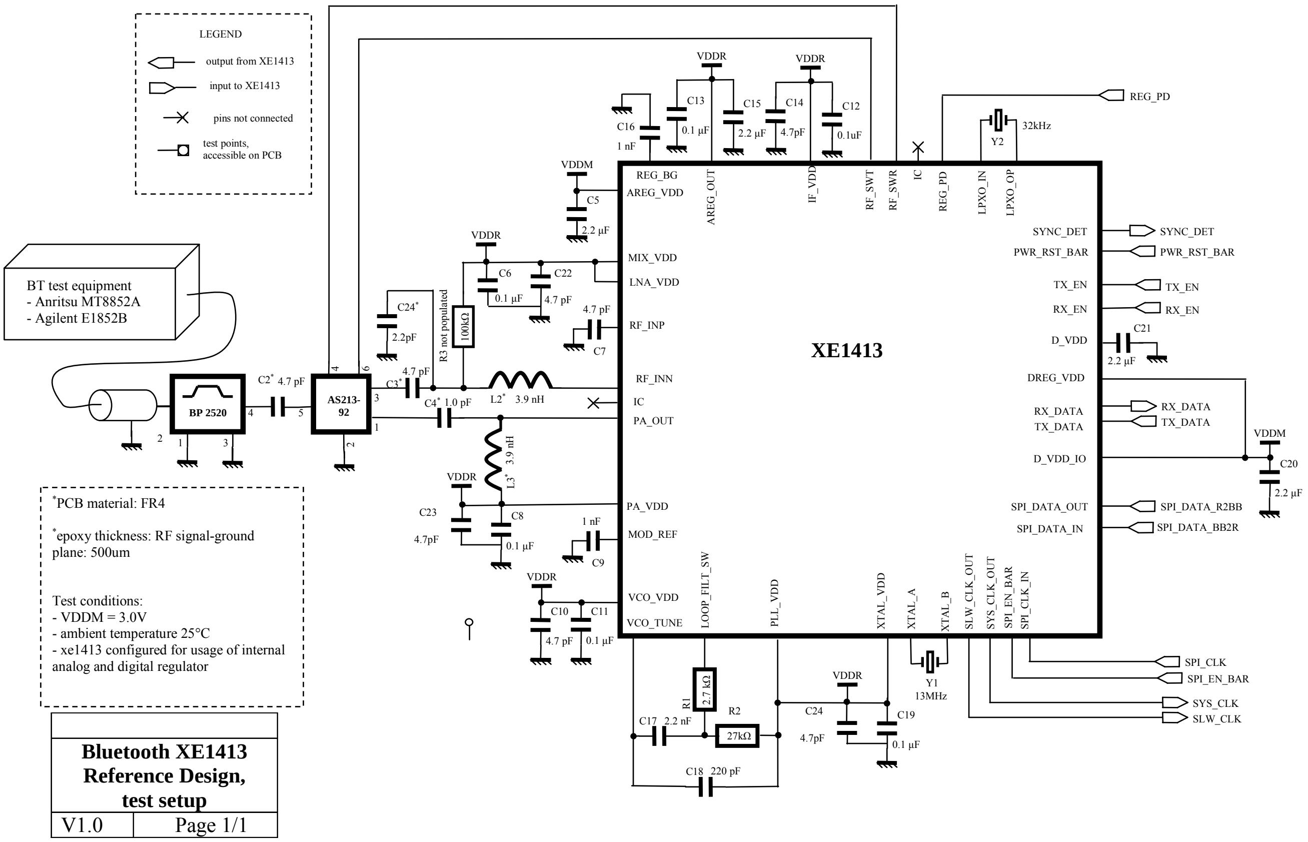
Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Receiver sensitivity at antenna input	PR0B	0.1% BER correlator-based STR		–85	–80	dBm
Receiver sensitivity degradation due to Bluetooth “dirty” transmitter		Bluetooth “dirty” transmitter definition			1	dB
Maximum input signal (desired or interferer)	PIMAX		–18	–16		dBm
C/I performance	C/I	BQTF Bluetooth v1.2 compliant				dB
Receiver latency, antenna to bits at pins of baseband device	TRX_LATENCY			4.6		µs
RSSI range	RSSI		–90		–40	dBm
RSSI absolute error for input signal < –40 dBm					6	dB
Receive data sampling rate	FDIGITIZATION			13		MHz
Current Drain (total A_VDD + D_VDD current) see Table 18 for state definitions						
Peak current drain during receive mode (D_VDD = 1.8 V)	IRECEIVE			26		mA
Peak current drain during receive mode (D_VDD = 1.5 V)	IRECEIVE			24		mA
Peak current drain during transmit mode, maximum transmit power	ITRANSMIT			19		mA
Peak current drain during transmit mode, –10 dBm transmit power	ITRANSMIT–10			11		mA
Inter-packet current (RX_EN and TX_EN low)	IINTER_PACKET			160		µA
Internal current drain with only 32 kHz crystal reference oscillator running	ISLEEP_LPXO_ACTIVE			15		µA
Current drain in power-down mode	IPOWERDOWN			3		µA
Crystal Oscillator						
MXTAL, main crystal oscillator	fCLK	Maximum ESR = 40 Ω, crystal loading capacitor specification = 10 pF; tolerance 10 ppm, external loading capacitors not required		13		MHz
External main oscillator drive levels (see Figure 2)	VMXTAL	AC coupling	0.3		XTAL_VDD	Vp-p
Crystal tuning range with 4-bit SPI programmability	13 MHz XtalTUNING		±20	±30	±40	ppm
LPXO, low power crystal oscillator	fLPXO	ESR = 50 kΩ nominal, crystal loading capacitor specification = 10 pF, external loading capacitors not required		32		kHz
External low power oscillator drive levels (see Figure 3)	VLPXO	AC coupling	50		750	mVp-p
Transmitter						
Transmit band			2.402		2.480	GHz

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Maximum transmit output power at antenna (see Figure *17*)	$P0_{HIGH}$		-4.0	0	2.5	dBm
Transmit power attenuation	$P0_{ATTENUATION}$		0		26	dB
Transmit power attenuation step size	$P0_{ATTEN\_STEP}$			2		dB
Transmitter spectral performance	P_{S}	BQTF Bluetooth v1.2 compliant				dBm
Transmitter latency, bits at baseband pins to signal at antenna	$T_{TX\_LATENCY}$			3.1		µs
Transmit data sampling rate	$F_{DIGITIZATION}$			1		MHz
SPI and Synchronization Detect Timing						
SPI clock period	t_{CLK}		100	200		ns
SPI data setup time	t_{DSU}		2			ns
SPI data hold time	t_{DHD}		1			ns
SPI enable to clock rising edge	t_{EN_CLK}		¼ tclk			ns
SPI clock falling edge to enable	t_{CLK_EN}		¼ tclk			ns
SPI clock duty cycle	t_{CKL} or t_{CKH}		0.4 t_{CLK}		0.6 t_{CLK}	ns
Synchronization detect pulse width			2/fmxtal			
Reset Pin Timing						
Power on reset output low time (interval that PWR_RST_BAR, pin 30, output drives low when VDD applied). See Figure 15.			35	50	65	ms
Soft reset (minimum low input interval to PWR_RST_BAR, pin 30, from baseband to reset XE1413)			10			µs

Table 17 - XE1413 Electrical Specifications
(VDD = 1.8 V, @ +25 ℃ unless otherwise specified)

States	Description
inter_packet	13 MHz MXTAL running. Radio waiting for assertion of RX_EN or TX_EN.
sleep_lpxo_active	Only 32 kHz LPXO running. Radio blocks, MXTAL, and RC oscillator are all powered down.
sleep_rc_active	Only 32 kHz RC oscillator running. Radio blocks, MXTAL, and LPXO are all powered down.
Power down	All radio blocks, MXTAL, LPXO, and RC oscillator are powered down.
Receive	Receiver outputting demodulated data on RX_DATA pin.
Transmit	Transmitting at selected output power on selected channel.

Table 18 - XE1413 State Definitions



*PCB material: FR4

*epoxy thickness: RF signal-ground plane: 500um

Test conditions:
- VDDM = 3.0V
- ambient temperature 25°C
- xe1413 configured for usage of internal analog and digital regulator

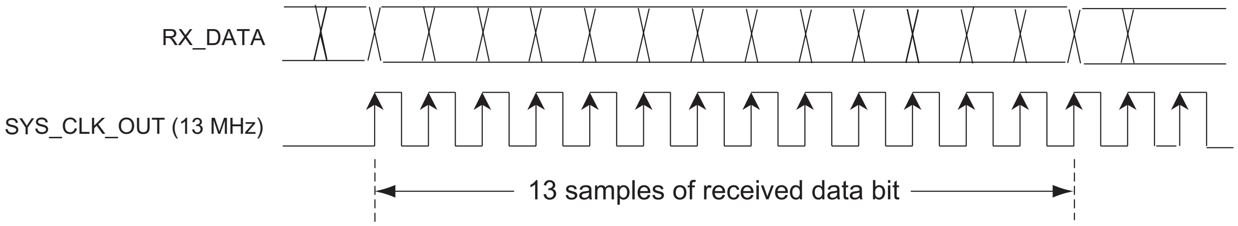
Bluetooth XE1413 Reference Design, test setup

V1.0	Page 1/1

Figure 17 - reference design, test setup

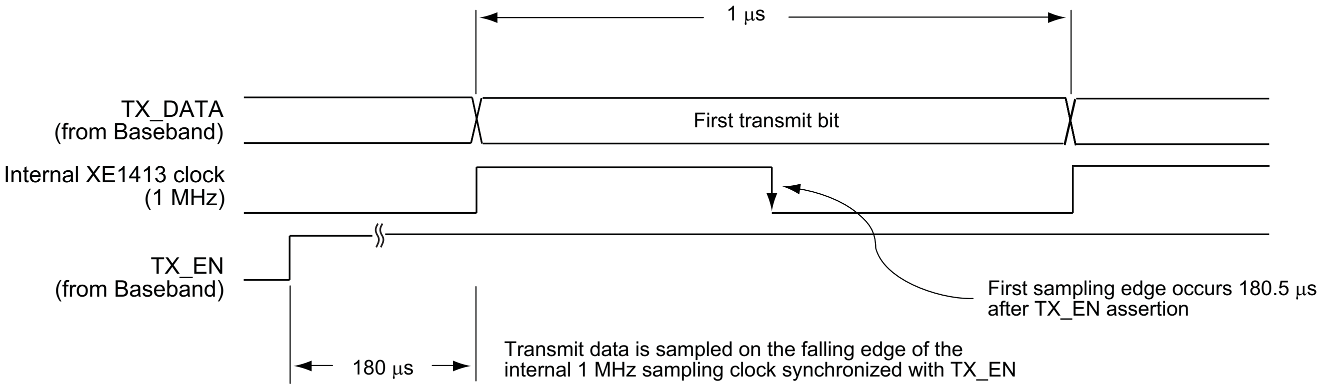
4.4 DATA RECEIVE AND TRANSMIT TIMING

Figure 18 and Figure 19 show the data receive and transmit timing diagrams, respectively.



Over sampled receive data transitions on the rising edge of SYS_CLK_OUT.
Baseband should sample receive data on the falling edge of SYS_CLK_OUT.

Figure 18 - RX_DATA vs. SYS_CLK_OUT Timing Diagram



First sampling edge occurs 180.5 µs after TX_EN assertion

Transmit data is sampled on the falling edge of the internal 1 MHz sampling clock synchronized with TX_EN

Figure 19 - TX_DATA vs. TX_EN Timing Diagram

5 APPLICATION DIAGRAM

The Figure 20 shows a block diagram for a Bluetooth headset using the XE1413 radio.

An application schematic for a Bluetooth headset solution using the XE1413 and Semtech baseband and application controller SX1441 is shown in Figure 21 and Figure 22.

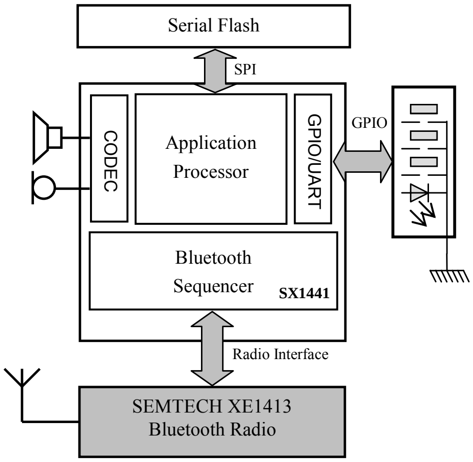


Figure 20 - XE1413 and Semtech Bluetooth Headset Solution Block Diagram

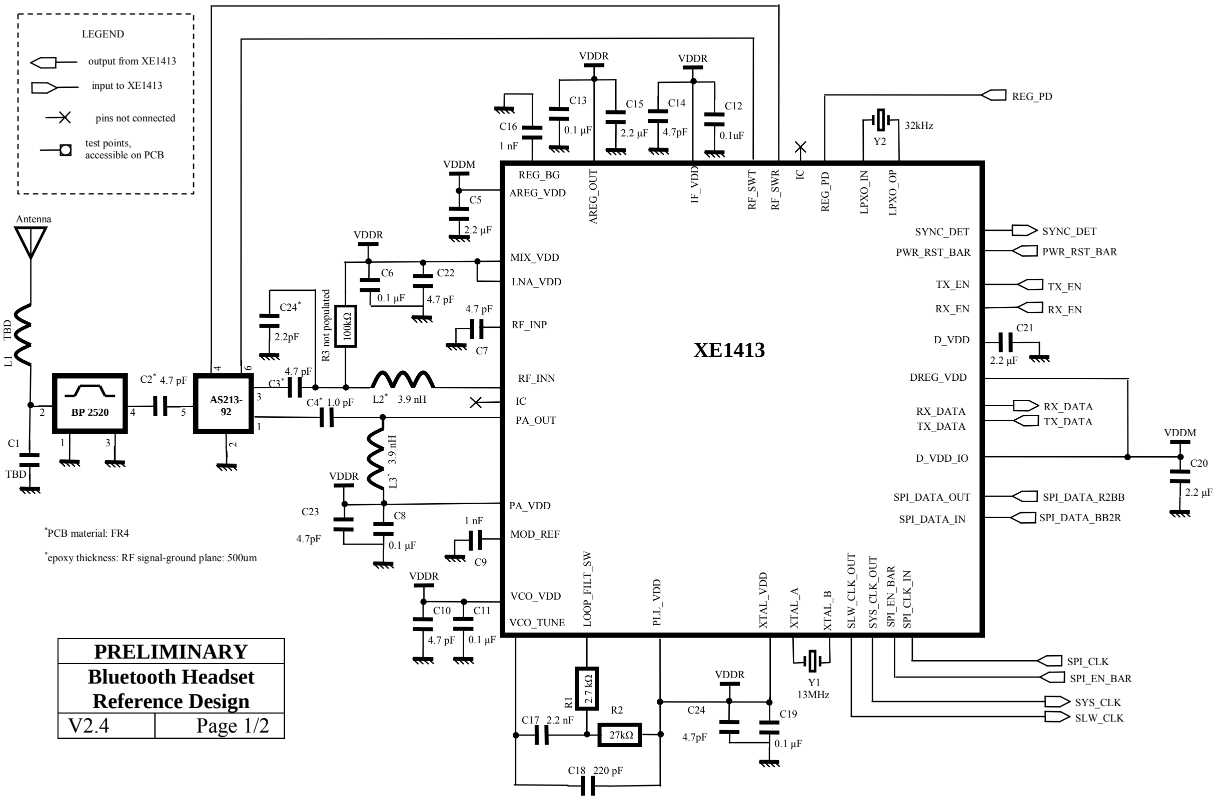


Figure 21 - headset schematic, page 1/2

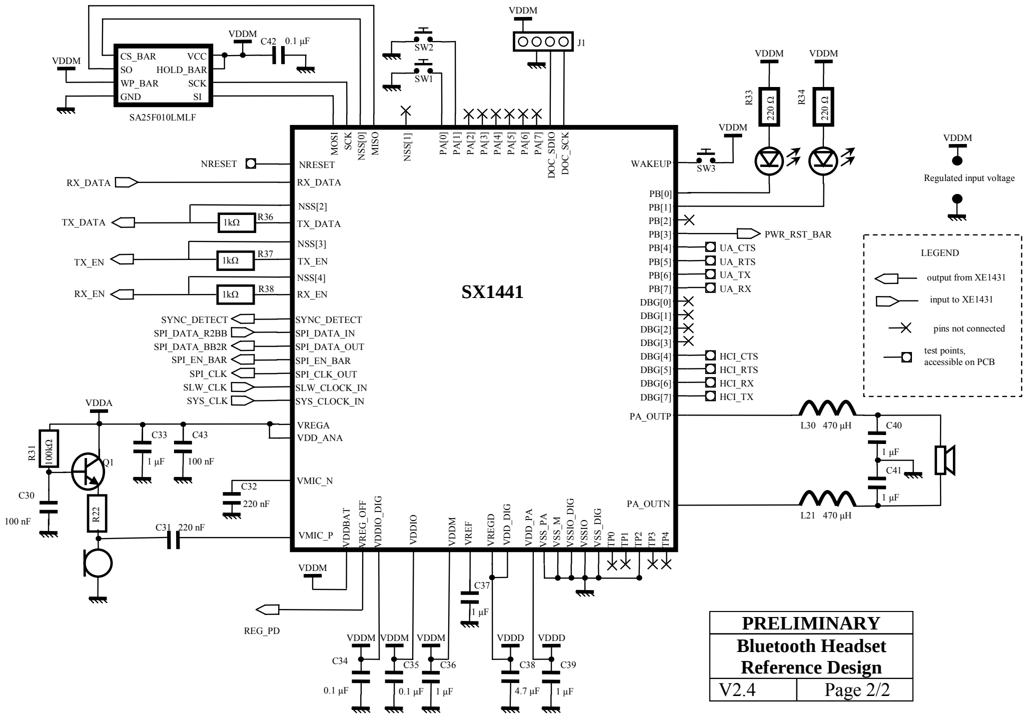


Figure 22 - headset schematic, page 2/2

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